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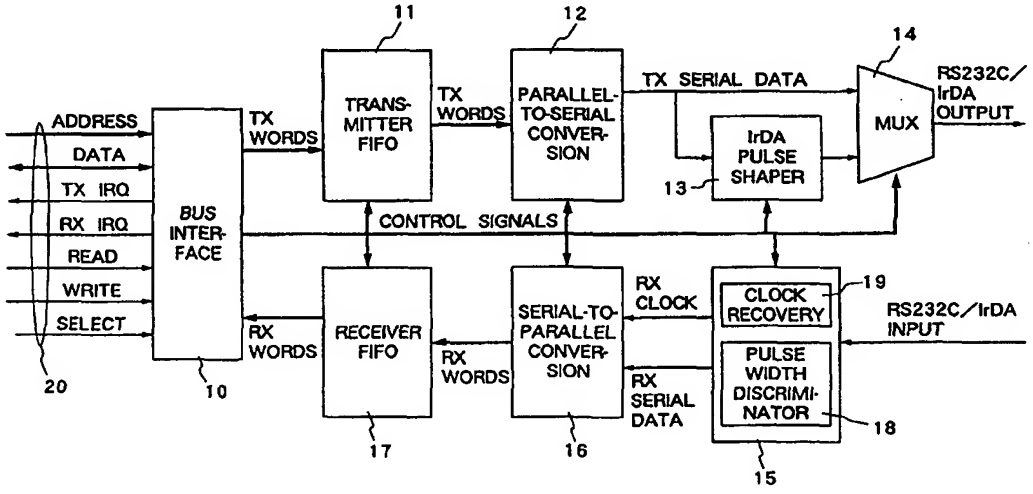

(57) Abstract

A multi–function UART (universal asynchronous receiver transmitter) for use in a data processing system, includes an interface (10) for connection to a host CPU bus (20); a transmitter FIFO (11) connected to the interface (10); a parallel–to–serial converter (12) connected to an output of the transmitter FIFO (11) to provide a serial data stream; a pulse shaper (13) for controlling the pulse length of each output pulse of the parallel–to–serial converter (12) according to value of the corresponding serial bit; output selector (14) for selecting one of outputs of the parallel–to–serial converter (12) and the pulse shaper (13); a receiver input stage (15) having a pulse width discriminator (18) and a clock recovery circuit (19); a serial–to–parallel converter (16) connected to an output of the receiver input stage; and a receiver FIFO buffer (17) connected between the serial–to–parallel converter (16) and the interface (10).

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DESCRIPTION

MULTI-FUNCTION UART

Technical Field

This invention relations to a multi-function UART (universal asynchronous receiver transmitter) intended for use in a data processing system, such as a personal computer.

Background Art

Where an infrared interface is required in a data processing system it is usually to employ a standard UART device in a form of an LSI (large scale integrated) circuit, which is usually "NS16550" UART by National Semiconductor Inc. or a "16550" compatible UART, and attach a separate IrDA (Infrared Data Association) modem, which is an infrared modem based on one of IrDA standards, to the transmit and receive lines. However, if the system also has a serial interface such as an RS232 interface the serial interface will also usually include a 16550 compatible UART. This duplication not only wastes space and money, but also substantially doubles the effort required for programming.

Disclosure of Invention

The object of the present invention is the provision of a multi-function UART so as to avoid duplication.

In accordance with the invention there is provided a multi-function UART for use in a data processing system,

comprising, an interface for connection to a host processor bus, a transmitter FIFO (first-in first-out) buffer connected to the interface, a parallel-to-serial converter connected to an output of the transmitter FIFO buffer to provide a serial data stream, a pulse shaper for controlling pulse length of each output pulse of the parallel-to-serial converter according to value of a corresponding serial bit, output selection means for selecting one of outputs of the parallel-to-serial converter and the pulse shaper, a receiver input stage including a pulse length discriminator and bit clock recovery means, a serial-to-parallel converter connected to an output of the receiver input stage, and a receiver FIFO buffer connected between the serial-to-parallel converter and the interface.

RS232 and IrDA interface functions can thus be included in a single device enabling considerable savings to be made.

Brief Description of Drawings

FIG. 1 is a block diagram of a multi-function UART in accordance with a preferred embodiment of the present invention; and

FIG. 2 is a block diagram showing a construction of the interface block.

Best Mode for Carrying out the Invention

The UART shown in FIG. 1 includes an interface block 10 for connection to the host CPU (central processing unit)

bus 20. The interface block receives address data, a read control signal, a write control signal and a chip select signal from the host CPU bus 20, and send a transmitter interrupt request (TX IRQ) and a receiver interrupt request (RX IRQ) to the host CPU bus 20 as well as it interchanges data with the host CPU bus 20.

As shown in FIG. 2, the interface 10 contains memory registers 21 to 30 which are all configuration registers for the UART. The memory registers includes a receiver buffer register (RBR) 21 storing a received byte, a transmitter holding register (THR) 22 holding a transmit byte, a FIFO (first-in first-out) status register (FSR) 23 indicating status of the transmitter and receiver FIFO buffers 11, 17, a FIFO control register (FCR) 24 for controlling FIFO buffers 11, 17, a line control register (LCR) 25 for setting a divisor latch access bit (DLAB) and parameters for asynchronous communication, a line status register (LSR) 26 indicating the status of the communication line, a pulse width register (PWR) 27 for setting a width of an IrDA transmit pulse, a baud rate prescaler (BRP) 28 including an IrDA enable bit and storing bits 3-0 of the baud rate divisor, a first divisor latch (DLL) 29 storing bits 11-4 of the baud rate divisor and a second divisor latch (DLM) 30 storing bits 19-12 of the baud rate divisor. Table 1 below shows the address, bit constitution and function of each of the memory registers 21 to 30.

Table 1

Address	Name	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 DLAB=0 (Read)	RBR	Receiver Buffer Register	Received Byte							
0 DLAB=0 (Write)	THR	Transmitter Holding Register	Transmit Byte							
1 DLAB=0		Unused	0x00							
2 (Read)	FSR	FIFO Status Register	FIFO enabled	FIFO enabled	0	0	0	0	0	0
2 (Write)	FCR	FIFO Control Register	Receiver Trigger Level		0	0	DMA Mode	XMIT FIFO Reset	RCV FIFO Reset	FIFO enable
3	LCR	Line Control Register	DLAB	0	0	Even Parity Select	Parity Enable	Stop Bits	Word Length Select	
4		Unused	0x00							
5	LSR	Line Status Register	Error in RCV FIFO	TX Empty	Holding Register Empty	0	Framing Error	Parity Error	Overrun Error	Data Ready
6	PWR	Pulse Width Register	0	0	IrDA Transmit Pulse Width					
7	BRP	Baud Rate Prescaler	0	0	Loop back Enable	IrDA Enable	Baud Rate divisor Fine Tune (bits 3-0 of divisor)			
0 DLAB=1	DLL	Divisor Latch (LSB)	Baud Rate Divisor Low Byte (bits 11-4 of divisor)							
1 DLAB=1	DLM	Divisor Latch (MSB)	Baud Rate Divisor High Byte (bits 19-12 of divisor)							

DMA: Direct Memory Access, XMIT, TX: Transmitter, RCV: Receiver, LSB: Least Significant Bit, MSB: Most Significant Bit, DLAB: Divisor Latch Access Bit.

The interface block 10 performs all address and select decoding for the UART.

The IrDA enable bit of the BRP register 28 is reset when the UART is to operate in a standard mode, that is, an RS232 serial transmission mode and the IrDA enable bit is set when the UART is to operate in an infrared mode, that is, an IrDA transmission mode.

On the transmission side, the UART includes a transmitter FIFO (first-in first-out) buffer 11 which receives data to be transmitted from the interface 10 as TX words and can store up to 16 bytes of the data. The output of the FIFO 11 is connected to a parallel-to-serial converter 12 which takes data one byte at a time from the transmitter FIFO 11, truncates them to the correct bit length specified by the LCR register 25 of the interface 10. The converter 12 also calculates the parity bit (if required) and adds start and stop bits. The converter 12 outputs a standard RS232 serial data stream as TX serial data at the baud rate specified by the BRP, DLL and DLM registers 28 to 30 of the interface 10.

An IrDA pulse shaper 13 operates on the data stream from the converter 12 to provide an IrDA compatible pulse train with short pulses for "0"s in the RS232 stream and longer pulses (of length defined by the value held in the PWR register 27 of the interface 10) for "1"s in the RS232 serial data stream. An output selector 14 controlled by the IrDA enable bit in the BRP register 28 of the interface

10 is connected to pass the output of either the converter 12 or the pulse shaper 13 to the final output terminal.

On the receiver side, there is a receiver input stage 15 which receives the input pulse stream and includes a pulse width discriminator 18 and a clock recovery circuit 19. This input stage 15 produces by a receive clock pulse for each pulse received and when an IrDA mode constructs an RS232 serial train from the received pulses in accordance with whether the received pulse lengths exceed the set IrDA pulse width. Concretely, in the IrDA mode, the input stage 15 outputs "0" for a received pulse having a length shorter than the predetermined length defined by the value held in the PWR register 27 of the interface 10 and outputs "1" for a received pulse longer than the predetermined length.

A serial to parallel converter 16 converts the serial data back into bytes based on the receive clock pulse and checks for correct framing and parity. The output of the converter 16 is passed to a receiver FIFO buffer 17. The receiver FIFO 17 is similar to the transmitter FIFO 11 in construction, but stores additional information for every byte stored representing the framing and parity error status checked by the converter 16.

It should be noted that in addition to the advantages already referred to above the UART also has the advantage of allowing RS232 and IrDA interfaces to share an IRQ and address which could be important in a personal computer application. Reduction of chip area and size are of more

importance in such applications as mobile telephone handsets.

CLAIMS

1. A multi-function UART (universal asynchronous receiver transmitter) for use in a data processing system, comprising:

an interface for connection to a host processor bus;

a transmitter FIFO (first-in first-out) buffer connected to the interface;

a parallel-to-serial converter connected to an output of the transmitter FIFO buffer to provide a serial data stream;

a pulse shaper for controlling pulse length of each output pulse of the parallel-to-serial converter according to value of a corresponding serial bit;

output selection means for selecting one of outputs of the parallel-to-serial converter and the pulse shaper;

a receiver input stage including a pulse length discriminator and bit clock recovery means;

a serial-to-parallel converter connected to an output of the receiver input stage; and

a receiver FIFO buffer connected between the serial-to-parallel converter and the interface.

2 A multi-function UART according to claim 1, wherein the interface includes memory registers which can be programmed in use with configuration data for use by the UART, and one of the memory registers including a portion to determine whether the UART is to operate in standard mode or infrared mode.

3. A multi-function UART according to claim 2, wherein one of the memory registers includes a portion to determine a duration of the pulse length.

4. A multi-function UART according to claim 2, wherein the pulse shaper provides a pulse having a first length for each bit of "0" in the serial data stream and a pulse having a second length for each bit of "1" in the serial data stream, the second length being longer than the first length.

5. A multi-function UART according to claim 4, wherein one of the memory registers includes a portion to determine the second length.

6. A multi-function UART according to claim 1, wherein the receiver input stage constructs an serial data train from received pulses thereto in accordance with whether a length of the received pulse exceeds a predetermined pulse width.

7. A multi-function UART according to claim 5, wherein the receiver input stage constructs an serial data train from received pulses thereto in accordance with whether a length of the received pulse exceeds the second length.

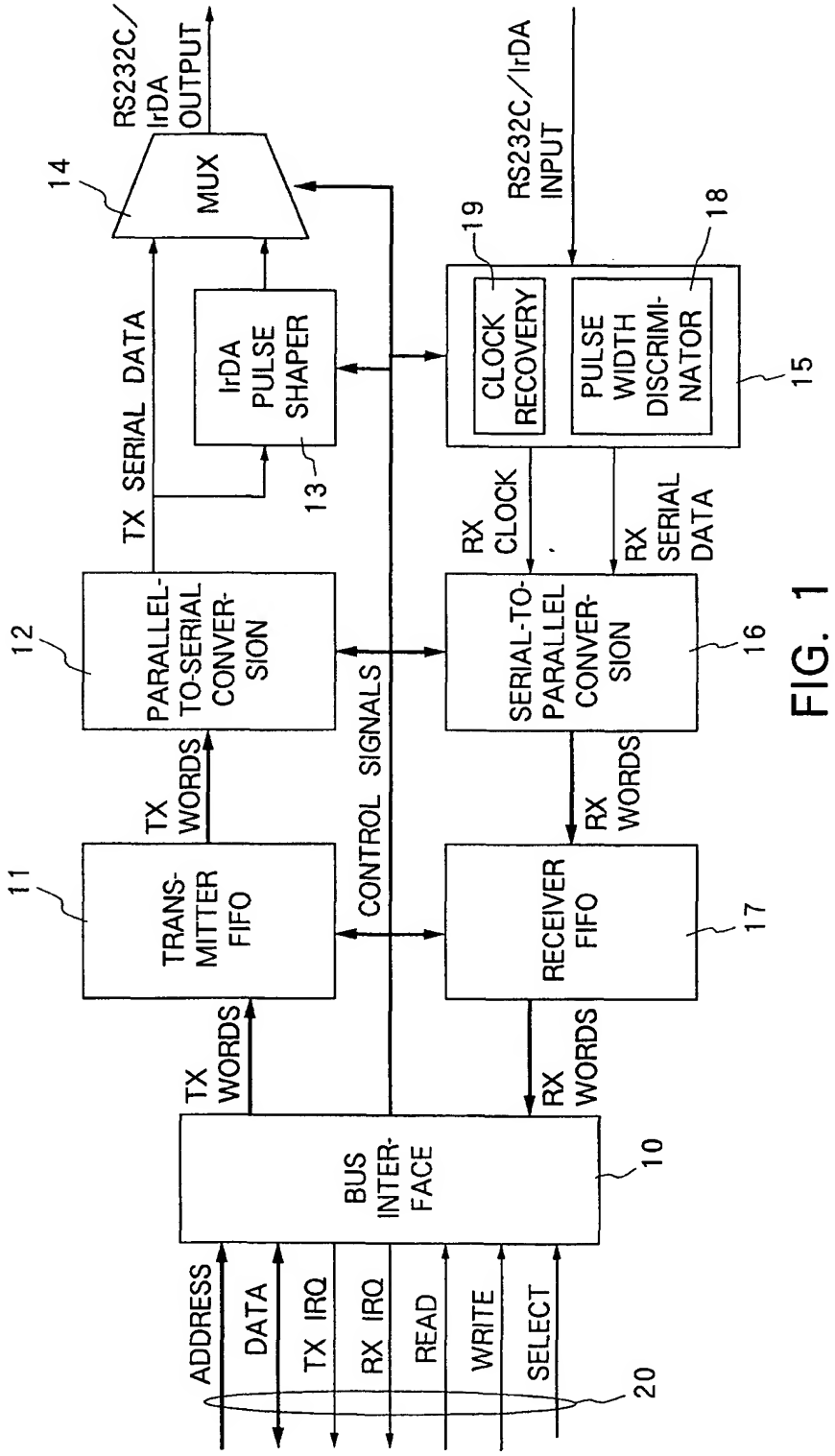
RS232C/IrDA OUTPUT
14
MUX
RS232C/IrDA INPUT
19
18
CLOCK RECOVERY
PULSE WIDTH DISCRIMI-NATOR
15
IrDA PULSE SHAPER
13
TX SERIAL DATA
RX CLOCK
RX SERIAL DATA
12
PARALLEL-TO-SERIAL CONVER-SION
SERIAL-TO-PARALLEL CONVER-SION
16
TX WORDS
RX WORDS
CONTROL SIGNALS
11
TRANS-MITTER FIFO
RECEIVER FIFO
17
TX WORDS
RX WORDS
BUS INTER-FACE
10
ADDRESS
DATA
TX IRQ
RX IRQ
READ
WRITE
SELECT
20

FIG. 1

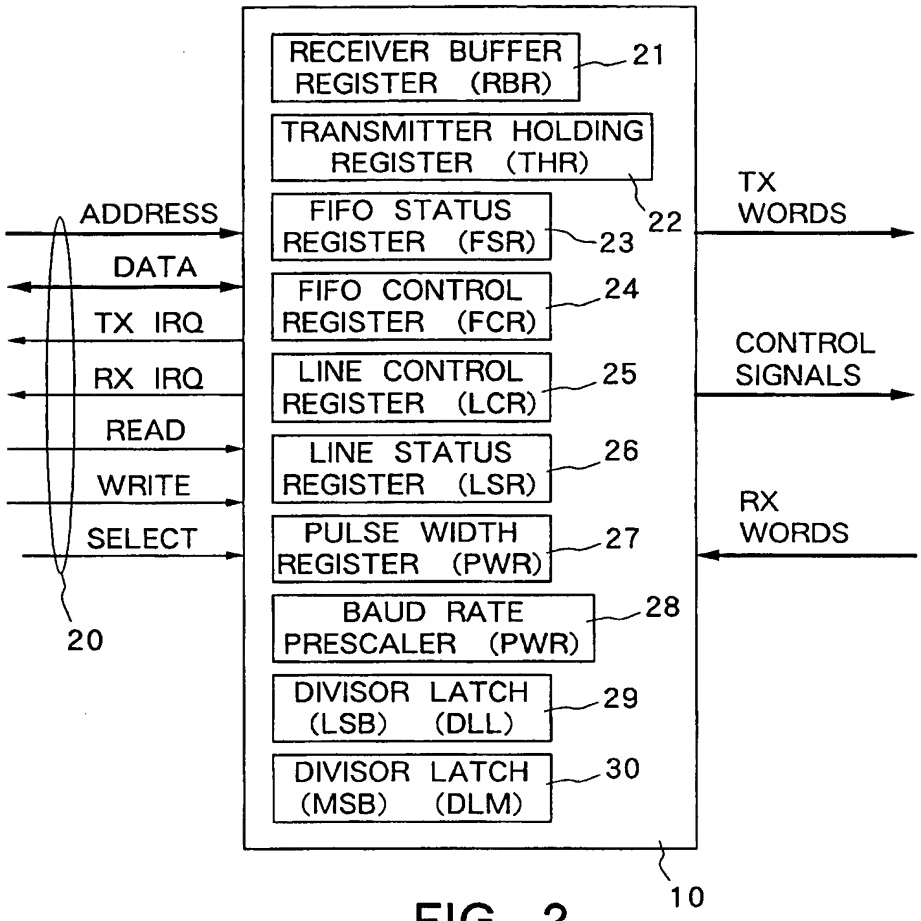
RECEIVER BUFFER REGISTER (RBR)
21
TRANSMITTER HOLDING REGISTER (THR)
22
FIFO STATUS REGISTER (FSR)
23
FIFO CONTROL REGISTER (FCR)
24
LINE CONTROL REGISTER (LCR)
25
LINE STATUS REGISTER (LSR)
26
PULSE WIDTH REGISTER (PWR)
27
BAUD RATE PRESCALER (PWR)
28
DIVISOR LATCH (LSB) (DLL)
29
DIVISOR LATCH (MSB) (DLM)
30
10
ADDRESS
DATA
TX IRQ
RX IRQ
READ
WRITE
SELECT
20
TX WORDS
CONTROL SIGNALS
RX WORDS

FIG. 2

INTERNATIONAL SEARCH REPORT

Internal Application No
PCT/JP 99/02376

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F13/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 557 751 A (BANMAN ET AL.) 17 September 1996 (1996-09-17) column 1, line 24 - line 56 column 3, line 65 -column 4, line 55 column 6, line 1 -column 9, line 3 column 11, line 3 -column 12, line 41; claims 2,6-8; figures 1-3,6,7	1-7
A	"New IC caps two decades of UART development" J JOURNAL, MAXIM ENGINEERING JOURNAL (UK), vol. 30, pages 3-10, XP002115829 IRN-1356-031X the whole document	1-7

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INTERNATIONAL SEARCH REPORT

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5557751 A	17-09-1996	EP 0665502 A	02-08-1995
		JP 7262111 A	13-10-1995